WHAT IS CLAIMED IS:

1. A serial communication device synchronizing with a synchronizing serial communication clock signal from an exterior device and communicating a communication data including a predetermined frames consisting of predetermined bits with a parity bit with an electronic circuit with respect to each bit comprising:

a monitor circuit synchronizing with the synchronizing serial communication clock signal and outputting a communication completion condition signal at a timing counted by the predetermined bit for the communication data; and

a check circuit for checking communication contents by the parity bit at a time synchronized with an output of the communication completion condition signal.

2. A serial communication device synchronizing with a synchronizing serial communication clock signal from an exterior device and communicating a communication data including predetermined frames consisting of a predetermined bits and a parity bit with an electronic circuit with respect to each bit comprising:

a monitor circuit synchronizing with the synchronizing serial communication clock signal and outputting a communication completion condition signal at a timing counted by a predetermined bit for the communication data; and

a check circuit for checking a communication contents by the parity bit at a timing synchronized the communication completion condition signal with the synchronized serial communication clock signal.

3. A serial communication device inputted an active signal and a synchronizing serial communication clock signal from an exterior device, and at a timing synchronized with the synchronizing serial communication clock signal under an active condition of the active signal and communicating a communication data including predetermined frames consisting of predetermined bits and a parity bit with an electronic circuit with respect to each bit comprising:

judging means for judging a switching condition of the active signal, and

checking means for checking a communication contents by the parity bit at a timing switching between the positive condition to the negative condition.

4. A serial communication device according to claim 3, wherein

the checking means checks the communication contents when the active signal changes from the active condition to the negative condition.